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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,717	12/15/2005	Freddy Roozeboom	NL 040226	8503

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EXAMINER	
CHEN, DAVID Z	

ART UNIT	PAPER NUMBER
2815	

NOTIFICATION DATE	DELIVERY MODE
03/04/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,717	ROOZEBOOM ET AL.	
	Examiner	Art Unit	
	David Z. Chen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8,10 and 20-27* is/are rejected.

7)☒ Claim(s) *2,4 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Amendment filed on February 03, 2011.

Specification

2. The title of the invention is broad and not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Electronic device, assembly and methods of manufacturing an electronic device comprising a vertical trench capacitor and a vertical interconnect.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 23 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,830,970 B2 to Gardes ("Gardes").

As to claim 23, Gardes discloses an electronic device comprising: a semiconductor substrate (11) having a first side and a second side; a plurality of trenches (21) on the first side of the substrate (11), each of the trenches (21) extending into the substrate (11) from the first side; conductive material (silicon, 25) lining each of the trenches (21); a vertical interconnect (25) that extends through the substrate (11)

from the first side to the second side, the vertical interconnect (25) having walls; a single deposition layer (24) of dielectric material on the first and second sides of the substrate (11), on the conductive material lining (silicon, 25) each of the trenches (21), and on the walls of the vertical interconnect (25) (See Fig. 2B, Fig. 2C, Fig. 2E, Column 2, lines 61-67, Column 3, lines 1-2, 24-63).

As to claim 25, Gardes further disclose wherein the vertical interconnect (25) includes a plurality of parallel trenches (See Fig. 3A).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,830,970 B2 to Gardes ("Gardes") as applied to claim 23 above, and further in view of U.S. Patent Application Publication No. 2001/0005046 A1 to Hsuan et al. ("Hsuan"). The teaching of Gardes has been discussed above.

As to claim 24, although Gardes discloses wherein the vertical interconnect (25) has a first part and a second part, the first part extending from the first side of the substrate (11) to the second part, the second part extending from the second side of the substrate (11) to the first part (See Fig. 2E), Gardes does not further disclose wherein the second part being wider than the first part.

However, Hsuan does disclose the second part (56, 58, 60) being wider than the first part (42) (See Fig. 2H, ¶ 0033, ¶ 0035, ¶ 0036).

In view of the teaching of Hsuan, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Gardes with the teaching of Hsuan to have the second part being wider than the first part because the wider part allows the interconnect to accommodate a bump and chips coupled by the bump have a shorter signal transmitting path and thus reducing electrical

impedance (See ¶ 0048).

As to claim 26, Gardes further discloses wherein the first part of the vertical interconnect (25) includes a plurality of parallel trenches (25) each of which extends from the first side of the substrate (11) to the second part of the vertical interconnect (25) (See Fig. 2E, Fig. 3A).

5. Claims 1, 3, 5-8, 10, 20-23, 25, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,030,481 B2 to Chudzik et al. ("Chudzik") in view of U.S. Patent No. 6,025,226 to Gambino et al. ("Gambino").

As to claim 1, although Chudzik discloses an electronic device comprising a semiconductor substrate (200) having a first side and a second side; a vertical trench capacitor (3010) including a plurality of trenches in which dielectric material (3020) is present between the first (3080) and second (3030) conductive surfaces; and a vertical interconnect (410') that extends through the substrate (200) from the first side to the second side, the vertical interconnect (410') being insulated from the substrate (200) by dielectric material (420') (See Fig. 3b, Fig. 3c, Fig. 4b, Fig. 4c, Fig. 4d, Column 4, lines 43-54, Column 6, lines 13-37) (Note: the vertical interconnect is used as decoupling capacitor by using a high dielectric constant insulator, as in the trench capacitor, in the via as the capacitor dielectric), Chudzik does not specifically disclose wherein the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer.

However, Gambino does disclose wherein the dielectric material (322) of the vertical interconnect (350) and the dielectric material (322) of the vertical trench

capacitor (360) being common material formed from a single deposition layer (322) (See Fig. 3, Fig. 6, Column 2, lines 36-42, Column 4, lines 5-15, Column 6, lines 18-53).

In view of the teaching of Gambino, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Chudzik with the teaching of Gambino to have wherein the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer because a single deposition layer eliminates the need for an additional step to pattern the dielectric layer (See Column 2, lines 36-42, Column 6, lines 48-53).

As to claim 3, Chudzik further discloses characterized in that the vertical interconnect (410') includes a plurality of parallel trenches (410') each of which is substantially filled with electrically conductive material (410') (See Column 6, lines 13-25, additional 410' structures).

As to claim 5, Chudzik further discloses wherein contact pads (270) for coupling to an external carrier are present on the second side; a first vertical interconnect (410') is used for grounding and a second interconnect (410') is used for signal transmission (See Fig. 3c, Fig. 4c, Column 6, lines 13-37).

Further regarding claim 5, while features of an apparatus may be recited either structurally or functionally (used for grounding, used for signal transmission), claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226,

228-29 (CCPA 1971); In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]ppratus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). The structures of the first vertical interconnect and second interconnect are met by Chudzik.

As to claim 6, Chudzik further discloses wherein the first (410') and second (410') vertical interconnect are designed so as to form a coaxial structure (See Fig. 4c).

As to claim 7, Chudzik further discloses wherein that an integrated circuit is defined on the second side of the substrate (200) (Column 4, lines 19-35).

As to claim 8, Chudzik further discloses wherein the substrate (200) comprises a high-ohmic zone which is present adjacent to the vertical capacitors (3010) and acts as a protection against parasitic currents (See Column 6, lines 41-67).

Further regarding claim 8, while features of an apparatus may be recited either structurally or functionally (acts as a protection against parasitic currents), claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]ppratus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). The structure of the high-ohmic zone is met by Chudzik.

As to claim 10, Chudzik discloses further comprising a semiconductor device

(102), which semiconductor device (102) is electrically connected to bond pads (270) present on the first side of the substrate (200) (See Fig. 4c, Column 4, lines 19-35).

As to claim 20, although Chudzik discloses the dielectric material (3020) of the vertical trench capacitor (3010) and the dielectric material (420') of the vertical interconnect (410'), Chudzik does not further disclose wherein the dielectric material of the vertical trench capacitor and the dielectric material of the vertical interconnect are formed by depositing a layer of dielectric material on the substrate and partially etching the deposited layer of the dielectric material.

However, Gambino does disclose wherein the dielectric material (322) of the vertical trench capacitor (360) and the dielectric material (322) of the vertical interconnect (350) are formed by depositing a layer (322) of dielectric material on the substrate and partially etching the deposited layer (322) of dielectric material (See Fig. 3, Fig. 6, Fig. 7, Column 2, lines 36-42, Column 4, lines 5-15, Column 6, lines 18-53).

In view of the teaching of Gambino, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Chudzik with the teaching of Gambino to have wherein the dielectric material of the vertical trench capacitor and the dielectric material of the vertical interconnect formed by depositing a layer of dielectric material on the substrate and partially etching the deposited layer of the dielectric material because a single deposition layer eliminates the need for an additional step to pattern the dielectric layer (See Column 2, lines 36-42, Column 6, lines 48-53).

As to claim 21, although Chudzik discloses the dielectric material (3020) of the

vertical trench capacitor (3010) and the dielectric material (420') of the vertical interconnect (410'), Chudzik does not further disclose wherein the dielectric material of the vertical trench capacitor and the dielectric material of the vertical interconnect are identical dielectric material formed from the single deposition layer.

However, Gambino does disclose wherein the dielectric material (322) of the vertical trench capacitor (360) and the dielectric material (322) of the vertical interconnect (350) are identical dielectric material formed from the single deposition layer (322) (See Fig. 3, Fig. 6, Fig. 7, Column 2, lines 36-42, Column 4, lines 5-15, Column 6, lines 18-53).

In view of the teaching of Gambino, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Chudzik with the teaching of Gambino to have wherein the dielectric material of the vertical trench capacitor and the dielectric material of the vertical interconnect being identical dielectric material formed from the single deposition layer because a single deposition layer eliminates the need for an additional step to pattern the dielectric layer (See Column 2, lines 36-42, Column 6, lines 48-53).

As to claim 22, although Chudzik discloses the vertical interconnect (410') is substantially filled with conductive material and the second (3030) conductive surface of the vertical trench capacitor (3010) (See Fig. 3c, Fig. 4c), Chudzik does not further disclose wherein the conductive material of the vertical interconnect and the second conductive surface of the vertical trench capacitor being formed from common material of a single deposition layer of conductive material.

However, Gambino does disclose wherein the conductive material (324) of the vertical interconnect (350) and the second conductive surface (324) of the vertical trench capacitor (360) being formed from common material of a single deposition layer (324) of conductive material (See Fig. 7, Fig. 8, Column 6, lines 54-67, Column 7, lines 1-4).

In view of the teaching of Gambino, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Chudzik with the teaching of Gambino to have wherein the conductive material of the vertical interconnect and the second conductive surface of the vertical trench capacitor being formed from common material of a single deposition layer of conductive material because a single deposition layer eliminates the need for an additional step to pattern the dielectric layer and the conductive layer that results in a cost saving process (See Column 2, lines 36-42, Column 6, lines 54-67, Column 7, lines 1-4).

As to claim 23, although Chudzik discloses an electronic device comprising a semiconductor substrate (200) having a first side and a second side; a plurality of trenches (3010) on the first side of the substrate (200), each of the trenches (3010) extending into the substrate (200) from the first side; conductive material (3080) lining each of the trenches (3010); a vertical interconnect (410') that extends through the substrate (200) from the first side to the second side, the vertical interconnect (410') having walls; being insulated from the substrate (200) by dielectric material (420') (See Fig. 3b, Fig. 3c, Fig. 4b, Fig. 4c, Fig. 4d, Column 4, lines 43-54, Column 6, lines 13-37) (Note: the vertical interconnect is used as decoupling capacitor by using a high

dielectric constant insulator, as in the trench capacitor, in the via as the capacitor dielectric), Chudzik does not specifically disclose a single deposition layer of dielectric material on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect.

However, Gambino does disclose a single deposition layer (322) of dielectric material on the first and second sides of the substrate, on the conductive material lining (310) of the trench, and on the walls of the vertical interconnect (350) (See Fig. 3, Fig. 6, Column 2, lines 36-42, Column 4, lines 5-15, Column 6, lines 18-53).

In view of the teaching of Gambino, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Chudzik with the teaching of Gambino to have a single deposition layer of dielectric material on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect because a single deposition layer eliminates the need for an additional step to pattern the dielectric layer (See Column 2, lines 36-42, Column 6, lines 48-53).

As to claim 25, Chudzik further discloses wherein the vertical interconnect (410') includes a plurality of parallel trenches (410', 210, 260) (See Column 5, lines 23-28, Column 6, lines 13-25).

As to claim 27, Chudzik further discloses wherein the plurality of trenches (3010) form a vertical trench capacitor (See Fig. 3c, Fig. 4c, Column 4, lines 43-54).

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,030,481 B2 to Chudzik et al. ("Chudzik") in view of U.S. Patent No.

6,830,970 B2 to Gardes ("Gardes").

As to claim 1, although Chudzik discloses an electronic device comprising a semiconductor substrate (200) having a first side and a second side; a vertical trench capacitor (3010) including a plurality of trenches in which dielectric material (3020) is present between the first (3080) and second (3030) conductive surfaces; and a vertical interconnect (410') that extends through the substrate (200) from the first side to the second side, the vertical interconnect (410') being insulated from the substrate (200) by dielectric material (420') (See Fig. 3b, Fig. 3c, Fig. 4b, Fig. 4c, Fig. 4d, Column 4, lines 43-54, Column 6, lines 13-37) (Note: the vertical interconnect is used as decoupling capacitor by using a high dielectric constant insulator, as in the trench capacitor, in the via as the capacitor dielectric), Chudzik does not specifically disclose wherein the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer.

However, Gardes does disclose wherein the dielectric material (24) of the vertical interconnect (25) and the dielectric material (24) of a plurality of trenches (21) being common material formed from a single deposition layer (24) (See Fig. 2B, Column 3, lines 24-38).

In view of the teaching of Gardes, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Chudzik with the teaching of Gardes to have wherein the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer because a single deposition layer

enables obtaining of a same insulator on the walls of the trenches and via and thus obtaining the same electric qualities. Further, it is not necessary to have an additional step of protection of one of the two structures (See Column 3, lines 24-38).

Allowable Subject Matter

7. Claims 2, 4, and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments filed on February 03, 2011 have been fully considered but they are not persuasive. Applicants argue "Therefore, the proposed corresponding structure fails to correspond at least to dielectric material on both the first and second sides of the substrate". This is not found persuasive because as clearly seen in Fig. 2C and Column 3, lines 24-28 of Gardes, the dielectric material 24 is on both the first and second sides of the substrate.

9. Applicants further argue "In this instance, the teaching away in the '481 reference is evidenced in the reference itself, which explicitly teaches away from the combination with the Gambino reference as asserted. Specifically, the '481 reference acknowledges the method of manufacture of vertical interconnects as described in the '481 reference but there is no clear way of modifying the structure as proposed". This is not found persuasive because Chudzik discloses forming the trench capacitors and the

interconnect is based on the ease of processing and the thermal budget. The trench capacitor may be preferred to be formed at a different step than the interconnect in the case where the high k insulator in the trench capacitor is not compatible with the conductors in the interconnect (See Column 5, lines 61-67, Column 6, lines 1-3). However, Chudzik also discloses a commonly owned U.S. Pat. No. 6,221,769 to Dhong et al. teaches a method of manufacturing vias or interconnects and the insulator in the trench capacitors can be made of silicon nitride and the conductive material for the electrode of the trench capacitor can be made of copper (See Column 4, lines 15-17, Column 5, lines 11-22). Dhong et al. also disclose the conductive material used as via is made of copper while the insulator is made of silicon nitride (See Fig. 2). When the materials used in the trench capacitors and the interconnect are identical, there should inherently not have any compatibility issue. Further in view of the motivation provided by Gambino, a single deposition layer should be conducted to eliminate the need for an additional step to pattern the dielectric layer.

10. Furthermore, Chudzik also discloses the vertical interconnect is used as decoupling capacitor by using a high dielectric constant insulator as in the trench capacitor (See Column 6, lines 13-25). When both the interconnect and the trench capacitors employ high k insulators and both are intended to be used as capacitors, there should inherently not have any compatibility issue when forming these structures. Further in view of the motivation provided by Gardes, a single deposition layer is conducted to obtain of a same insulator on the walls of the trenches and via and thus

obtaining the same electric qualities. Further, it is not necessary to have an additional step of protection of one of the two structures.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Z. Chen whose telephone number is (571) 270-7438. The examiner can normally be reached on Monday-Friday 8:00 AM-4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eugene Lee/
Primary Examiner, Art Unit 2815

/D. Z. C./
Examiner, Art Unit 2815